AMENDMENTS TO THE CLAIMS

1. (Original) A method for flexibly nesting JTAG TAP controllers for IP cores in a FPGA-based system-on-chip (SoC), the method comprising:

selecting at least one available bit from a selectable bit register of a host JTAG TAP controller, said selectable bit register having a plurality of available bits; and

extending an apparent length of an instruction register of said host JTAG TAP controller by using said at least one available bit from said selectable bit register.

2. (Original) The method according to claim 1, further comprising the step of choosing at least one IP core JTAG TAP controller from a plurality of IP core JTAG TAP controllers nested in the FPGA-based SoC, said chosen at least one IP core JTAG TAP controller becoming communicably accessible by said host JTAG TAP controller.

3. (Original) The method according to claim 1, wherein said step of extending is done to emulate an instruction register of an IP core before configuration of an FPGA on the SoC.

4. (Original) The method according to claim 2, further comprising the step of shifting an instruction for said chosen at least one IP core JTAG TAP controller through said instruction register having said extended length, said shifted instruction causing said chosen at least one IP core JTAG TAP controller to execute said instruction.

5. (Original) The method according to claim 1, wherein said selecting step further comprises manually selecting said at least one available bit from said selectable bit register.

6. (Original) The method according to claim 1, wherein said selecting step further comprises programmably selecting said at least one available bit from said selectable bit register.

7. (Currently Amended) A method for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC, the method comprising:

choosing at least one IP core JTAG TAP controller from a plurality of JTAG TAP controllers nested in the FPGA-based SoC; [[and]]

programmably connecting said selected at least one IP core JTAG TAP controller to a host JTAG TAP controller; and

selecting an apparent register size based upon a number of IP cores implemented in the FPGA-based SoC.

8. (Currently Amended) The method according to claim 7, ~~further comprising the~~ wherein the step of selecting the apparent register size comprises a step of selecting at least one bit from a selectable bit register of said host JTAG TAP controller, said selectable bit register having a plurality of available bits.

9. (Original) The method according to claim 8, further comprising extending an apparent length of an instruction register of said host JTAG TAP controller, said apparent length of said instruction register including a combined length of said at least one bit from said selectable bit register and said bits comprising said instruction register.

10. (Original) The method according to claim 9, further comprising the step of shifting an instruction through said instruction register having said combined length, said shifted instruction for causing the instruction to be executed in said JTAG TAP controller of said chosen IP core JTAG TAP controller.

11. (Original) A system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC, the system comprising:

a selectable bit register in a host JTAG TAP controller comprising at least one available bit; and

a selector for selecting said at least one available bit, said selector extending an apparent length of an instruction register of said host JTAG TAP controller by using said selected at least one available bit from said selectable bit register.

12. (Original) The system according to claim 11, further comprising a multiplexer for choosing at least one IP core JTAG TAP controller from a plurality of IP core JTAG TAP controllers nested in the FPGA-based SoC, said chosen at least one IP core JTAG TAP controller becoming communicably accessible by said host JTAG TAP controller.

13. (Original) The system according to claim 12, further comprising a shift circuit for shifting an instruction for said chosen at least one IP core JTAG TAP controller through said selected instruction register having said extended length, said shifted instruction causing said chosen at least one IP core JTAG TAP controller to execute said instruction.

14. (Currently Amended) A system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC, the system comprising:

a selector for choosing at least one IP core JTAG TAP controller from a plurality of JTAG TAP controllers nested in the FPGA-based SoC; [[and]]

a multiplexer for programmably connecting said at least one IP core JTAG TAP controller to a host JTAG TAP controller; and

an instruction register size select signal enabling the selection of an apparent register size to accommodate a variable number IP cores.

15. (Original) The system according to claim 14, further comprising a selectable bit register for said host JTAG TAP controller, said selectable bit register having at least one bit available for selection.

16. (Original) The system according to claim 15, wherein said selectable bit register extends an apparent length of an instruction register of said host JTAG TAP controller, said apparent length of said instruction register including a combined length of said at least one bit from said selectable bit register and said bits comprising said instruction register.

17. (Original) The system according to claim 16, further comprising a shifting circuit for shifting an instruction through said instruction register having said combined length, said shifted instruction for causing an instruction execution in said chosen IP core JTAG TAP controller.

18. (Original) A method for ensuring an information register length for nested JTAG TAP controllers for IP cores remains the same before and after a configuration of an FPGA in an FPGA-based system-on-chip (SoC), the method comprising:

forming instruction registers for the IP cores that are in series with the instruction registers of the FPGA of the SoC;

forming connections between FPGA JTAG logic of the FPGA and IP Core JTAG logic of the IP core using a programmable interconnect; and

emulating an instruction register of the IP core prior to configuration of the FPGA using a shift register of the same length as the instruction register of the IP core.

19. (Original) The method of claim 18, wherein the method further comprises the step of selectably accessing the nested JTAG TAP controllers of the IP cores via a programmable

input/output (IO).

20. (Original) The method of claim 18, wherein the step of emulating comprises the step of selectably varying the size of the shift register based on the number of IP cores in a given configuration of the SoC.

21. (Currently Amended) A system for performing boundary scan functions on a plurality of IP cores, the system comprising:

an FPGA-based system-on-chip (SoC) comprising a plurality of IP cores each including a first JTAG TAP controller; and

a host JTAG TAP controller coupled to each of the first JTAG TAP controllers, said host JTAG TAP controller comprising a selectable bit register enabling the selection of an apparent register size to accommodate a variable number of IP cores.

22. (Previously Presented) The system of Claim 21, wherein the FPGA-based SoC includes the host JTAG TAP controller.

23. (Previously Presented) The system of Claim 21, further comprising:

a selector circuit coupled between the first JTAG TAP controllers and the host JTAG TAP controller.

24. (Previously Presented) The system of Claim 23, wherein the FPGA-based SoC includes the host JTAG TAP controller and the selector circuit.

25. (Currently Amended) The system of Claim 21, wherein the ~~host JTAG TAP controller comprises:~~

[[a]] selectable bit register ~~having~~ comprises an input terminal coupled to the selector circuit and ~~further having~~ an output terminal providing a selected bit; and

and wherein the host JTAG TAP controller comprises an instruction register having an input terminal coupled to the output terminal of the selectable bit register, the instruction

register having an output terminal providing an instruction having an apparently extended length.

26. (Previously Presented) The system of Claim 25, further comprising:

a selector circuit coupled between the first JTAG TAP controllers and the host JTAG TAP controller.

27. (Previously Presented) The system of Claim 25, wherein the FPGA-based SoC includes the host JTAG TAP controller.